WHAT IS CLAIMED IS:

1. A method of image scaling using an array of processing elements, wherein the processing elements are arranged from a first processing element to an nth processing element, and wherein the image scaling uses a tap window size of N_{taps}, the method comprising:

(a) loading a frame buffer with pixel values from a video line, the pixel values in the loaded frame buffer being arranged into words having a width of n input pixel values; and

(b) broadcasting N_{taps} words from the loaded frame buffer to the array, wherein for each word, the input pixel values are arranged from a first input pixel value to an nth input pixel value such that, for each word broadcast to the array, the first processing element processes the first input pixel value in the word, the second processing element processes the second input pixel value in the word, and so on, and wherein the broadcast order of the pixel values is such that each processing element is configured to process the N_{Taps} input pixels it receives from the frame buffer into a scaled output pixel value using the same multiply-and-accumulate coefficient set, the processing elements thereby producing an output word of n scaled pixel values.

2. The method of claim 1, further comprising:

vertically-scaling pixels from a set of video lines to produce scaled pixel values for the video line, wherein the pixel values loaded into the frame buffer in act (a) are the vertically-scaled pixel values, and wherein the scaled output pixel values from each

processing element in act (b) are both horizontally-scaled and vertically-scaled output pixel values.

3. The method of claim 1, further comprising:

(c) repeating act (b) to produce a succession of output words from the array of processing elements, wherein the succession of output words represents a horizontally-scaled version of the video line.

4. The method of claim 3, further comprising:

repeating acts(a) through (c) to produce a succession of output words for a plurality of horizontally-scaled video lines;

storing the output words in the frame buffer for the plurality of scaled video lines

successively broadcasting sets of pixel values from the plurality of scaled video lines stored in the frame buffer to the array of processing elements; and

processing the sets of pixel values in the array of processing elements to produce a set of vertically-scaled output words.

5. The method of claim 4, further comprising:

re-ordering the vertically-scaled output words to provide a horizontally and vertically scaled video line.

6. The method of claim 1, wherein the number of input pixel values in the video line is an integer multiple N_i of n, and wherein the number of output pixel values in a scaled

video line is an integer multiple N_h of n, the broadcast order in act (b) being every N_ith input pixel, the scaled output pixel values from each multiply-and-accumulate calculation cycle being spaced apart by N_h pixel values.

7. The method of claim 1, wherein the number of input pixel values in the video line is not an integer multiple of n.

8. The method of claim 4, wherein the number of output pixel values in each scaled video line is not an integer multiple of n.

9. The method of claim 1, further comprising:

loading the frame buffer with padded video lines comprised of zero values, wherein when act (b) calculates output pixel values using input pixel values that are outside of the video line, zero values from the padded video lines are used.

10. An image processor, comprising:

an array of processing elements arranged from a first processing element to an nth processing element;

a frame buffer storing input words of n pixel values in length, the image processor being configured such that input words from the frame buffer may be successively broadcast to the array of processing elements, wherein the first processing element receives the first pixel value from a broadcast input word, the second processing element receives the second pixel value from the broadcast input word, and so on, the processing

elements being configured to perform multiply-and-accumulate (MAC) operations on the received values such that after the broadcast of N_{taps} words from the frame buffer, each processing element may provide a scaled output pixel value using the same MAC coefficient set, the array of processing elements thereby producing an output word of n scaled output pixel values.

11. The image processor of claim 10, wherein the image processor is configured such that the output word may be stored in the frame buffer.

12. The image processor of claim 10, wherein the output word is a horizontally-scaled output word.

13. The image processor of claim 10, wherein the output word is a vertically-scaled output word.

14. The image processor of claim 10, wherein the input words are vertically-scaled words and the output words are both horizontally and vertically scaled words.

15. The image processor of claim 10, wherein the input words are horizontally-scaled words and the output words are both horizontally and vertically scaled words.

16. The image processor of claim 10, further comprising one or more additional arrays of processing elements, the frame buffer being arranged to successively broadcast

input words to the one or more additional arrays such that the one or more additional arrays may also each provide an output word of scaled pixel values, wherein each scaled pixel value in the output word from the one or more additional arrays is calculated using the same multiply-and-accumulate coefficient set.

17. The image processor of claim 10, wherein the processing elements are reconfigurable processing elements.